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(54) Method for fabricating multi-level interconnection structure for semiconductor device.

(57) A method for fabricating a semiconductor device includes the steps of forming an interconnect metal film (33) on an insulating layer (32) and forming, on a surface of the interconnect metal film, a first insulating film (34) formed of P-SiN. The first insulating film (34) and the interconnect metal film (33) are simultaneously patterned to form a lower interconnect (33A). On the resulting surface, a second insulating film (35) having a polishing rate higher than that of the first insulating film (34) is formed. The entire surface of the second insulating film (35) is flattened by a chemical mechanical polishing process using the first insulating film (34) as a stopper. Then, on the resulting surface, a third insulating film (36) is formed. According to one embodiment, the first insulating film (34) used as the stopper remains on the lower interconnect (33A) but not between adjacent interconnects and, according to another embodiment, such film (34) is completely removed by etching. Thus, an increase in the capacitance between the interconnects is prevented and any stress migration therein is suppressed.

FIG. 3A

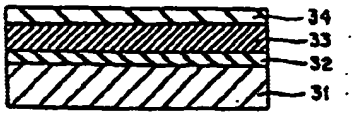


FIG. 3B

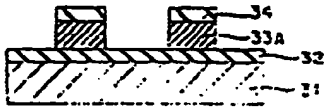


FIG. 3C

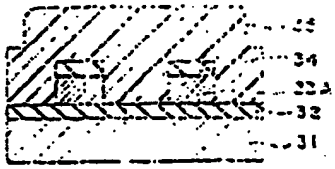


FIG. 3D

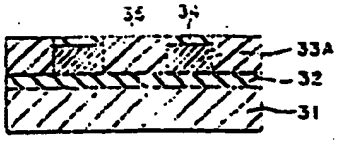
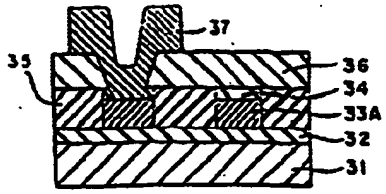


FIG. 3E



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BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to a method for fabricating a semiconductor device, and more particularly to a method for fabricating a semiconductor device in which an interlayer insulating film in a multi-level interconnection structure is flattened or planarized.

(2) Description of the Related Art

With an increased need for highly dense multi-level interconnections in a semiconductor device, there is a stronger requirement for an interlayer insulating film formed between metal interconnect layers to be perfectly flat and planar. In an attempt to meet such requirement, there has been proposed a method whereby a surface of the interlayer insulating film is polished by a Chemical Mechanical Polishing process (hereinafter referred to as "CMP process") which is a mechanical polishing process using a chemical agent. Figs. 1A through 1D are for showing an example of such process. Fig. 1A shows a state in which, after an aluminum interconnect layer 13 is formed in a predetermined pattern as a lower interconnect layer on a surface of an insulating film 12 on a semiconductor substrate 11, a plasma silicon oxide film (hereinafter referred to as "P-SiO film") 14 is formed as an interlayer insulating film. Then, the P-SiO film 14 is subjected to polishing of the CMP process and its surface is made flat as shown in Fig. 1B. Thereafter, though not shown in the drawings, an aluminum interconnect layer is formed as an upper interconnect layer and this completes the fabrication of a multi-level interconnect structure.

In a surface planarization technique using the CMP process, it is necessary that the polishing or lapping of the P-SiO film 14 be stopped at an exact timing when it has reached a certain predetermined thickness. However, it is difficult to know and determine the exact timing for stopping the polishing. If the amount of the polishing is excessive, the lower aluminum film 13 may be polished thereby reducing the thickness thereof as seen in Fig. 1C. On the contrary, if the amount of the polishing falls short, the P-SiO film 14 becomes too thick, as seen in Fig. 1D, in which case a step or uneven surface topography is not satisfactorily removed with a result that the surface planarization is insufficient.

In the conventional method described above, it has been the practice to determine the amount of polishing from the time converted and calculated from the polishing rate of the insulating film concerned. This involves a problem in that no appropriat polishing can be achieved when there is a change in the polishing rate itself.

As a way to solve the above problem, there has been proposed a surface planarization technique which utilizes an insulating film having a low polishing rate. That is, as shown in Fig. 2A, after an aluminum interconnect layer 23 is formed in a predetermined pattern as a lower interconnect on a surface of an insulating film 22 on a semiconductor substrate 21, a plasma silicon nitride film (hereinafter referred to as "P-SiN film") 24 as an interlayer insulating film having a low polishing rate is deposited to a thickness of about 0.3 µm by a Plasma-assisted Chemical Vapor Deposition (PCVD) on the overall surface of the device. Then, the P-SiO film 25 is deposited to a thickness of about 1.5 µm on the P-SiN film 24 by the PCVD process.

Thereafter, as shown in Fig. 2B, the overall surface of the resulting films is polished. The polishing rate of the P-SiN film 24 then is about 1/5 that of the P-SiO film 25 so that, when the polishing reaches a point where the P-SiN film 24 exposes its portion having a step therein, the overall polishing rate is lowered. For this reason, even when there is a slight error in the polishing time, it is possible to avoid the exposure and polishing of the aluminum interconnect layer 23 caused by the extended polishing time.

As shown in Fig. 2C, on the entire surface planarized as described above, a P-SiO film 26 is deposited to a thickness of about 0.8 µm to form an interlayer insulating film. Then, as shown in Fig. 2D, this interlayer insulating film 26 is provided with a throughhole and an upper aluminum pattern 27 is formed thereon and this completes the multi-level interconnect structure.

In the above described surface planarization technique, the P-SiN film 24 is utilized as a stopper when the P-SiO film 25 is polished by the CMP process. The use of the P-SiN film as a stopper in this way has been disclosed, for example, in Japanese Patent Application Kokai Publication No. Sho 62-216344 and Kokai Publication No. Sho 63-207153. However, the examples disclosed in these publications relate to the use of the P-SiN film as a stopper when a metal is polished.

Thus, conventionally, for making the interlayer insulating film flat, the P-SiN film has been used as a stopper in the CMP process. However, since the P-SiN film is formed in the entire surface area that includes the aluminum interconnects, the P-SiN film remains between adjacent interconnects after the completion of the multi-level interconnect structure. The dielectric constant of the P-SiN film is as large as about 6 so that line capacitance between the interconnects in the completed interconnect structure becomes large accordingly, and this possibly results in the deterioration of operation char-